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Method Of Forming Non-Volatile Resistance Variable Devices And Method Of Forming A Programmable Memory Cell Of Memory Circuitry

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Method Of Forming Non-Volatile Resistance Variable Devices And Method Of Forming A Programmable Memory Cell Of Memory Circuitry

TECHNICAL FIELD

This invention relates to methods of forming non-volatile resistance variable devices and to methods of forming a programmable memory cell of memory circuitry.

BACKGROUND OF THE INVENTION

Semiconductor fabrication continues to strive to make individual electronic components smaller and smaller, resulting in ever denser integrated circuitry. One type of integrated circuitry comprises memory circuitry where information is stored in the form of binary data. The circuitry can be fabricated such that the data is volatile or non-volatile. Volatile storing memory devices result in loss of data when power is interrupted. Non-volatile memory circuitry retains the stored data even when power is interrupted.

This invention was principally motivated in making improvements to the design and operation of memory circuitry disclosed in the Kozicki et al. U.S. Patent Nos. 5,761,115; 5,896,312; 5,914,893; and 6,084,796, which ultimately resulted from U.S. Patent Application Serial No. 08/652,706, filed on May 30, 1996, disclosing what is referred to as a programmable metallization cell. Such a cell includes opposing electrodes having an insulating dielectric material received therebetween. Received within the dielectric material is a fast ion

conductor material. The resistance of such material can be changed between highly insulative and highly conductive states. In its normal high resistive state, to perform a write operation, a voltage potential is applied to a certain one of the electrodes, with the other of the electrode being held at zero voltage or ground. The electrode having the voltage applied thereto functions as an anode, while the electrode held at zero or ground functions as a cathode. The nature of the fast ion conductor material is such that it undergoes a structural change at a certain applied voltage. With such voltage applied, a conductive dendrite or filament extends between the electrodes, effectively interconnecting the top and bottom electrodes to electrically short them together.

Once this occurs, dendrite growth stops, and is retained when the voltage potentials are removed. Such can effectively result in the resistance of the mass of fast ion conductor material between electrodes dropping by a factor of 1,000. Such material can be returned to its highly resistive state by reversing the voltage potential between the anode and cathode, whereby the filament disappears. Again, the highly resistive state is maintained once the reverse voltage potentials are removed. Accordingly, such a device can, for example, function as a programmable memory cell of memory circuitry.

The preferred resistance variable material received between the electrodes typically and preferably comprises a chalcogenide material having metal ions diffused therein. A specific example is germanium selenide having silver ions diffused therein. The present method of providing the silver ions within the germanium selenide material is to initially chemical vapor deposit the germanium

selenide glass without any silver being received therein. A thin layer of silver is thereafter deposited upon the glass, for example by sputtering, physical vapor deposition or other technique. An exemplary thickness is 200 Angstroms or less. The layer of silver is irradiated, preferably with electromagnetic energy at a wavelength less than 500 nanometers. The thin nature of the deposited silver enables such energy to pass through the silver to the silver/glass interface effective to break a chalcogenide bond of the chalcogenide material. This may form Ag_2Se, which effectively dopes the glass with silver. The applied energy and overlying silver ultimately result in the silver migrating into the glass layer such that a typical homogenous distribution of silver throughout the layer is achieved.

Saturation of silver in germanium selenide is apparently at a maximum of about 34 atomic percent or less depending on the germanium selenide stoichiometry. Yet, preferred existing technology for cell fabrication constitutes a concentration which is less than the maximum; in the case of 34 atomic percent maximum, an example concentration would be about 27 atomic percent.

After the chalcogenide material is provided with silver to a desired concentration, the top electrode material (typically silver) is next deposited. But, as the silver doping/diffusion into the chalcogenide material approaches the maximum or saturation, some Ag_2Se was discovered to form at the surface and remain there as opposed to diffusing into the glass. Further, the surface Ag_2Se was typically in the form of semicircular nodules or bumps anywhere from 50 Angstroms to 20 microns across. Unfortunately when the typical silver

electrode material is subsequently deposited, such tends to mound on top of these previous bumps. This can create voids to the doped germanium glass through the top electrode material, whereby the silver doped germanium selenide glass is partially exposed. Unfortunately, some of the photodeveloper solutions typically used for patterning the top electrode (i.e. tetramethyl ammonium hydroxide) will etch the glass that is exposed.

It would be desirable to overcome or at least reduce this problem. While the invention was principally motivated in overcoming this problem, it is in no way so limited. The artisan will appreciate applicability of the invention in other aspects unrelated to the problem, with the invention only being limited by the accompanying claims as literally worded and as appropriately interpreted in accordance with the doctrine of equivalents.

SUMMARY

The invention includes methods of forming a programmable memory cell of memory circuitry and non-volatile resistance variable devices. In one implementation, a method of forming a non-volatile resistance variable device includes forming a first conductive electrode material on a substrate. Chalcogenide comprising material is formed over the first conductive electrode material. The chalcogenide material comprises A_xSe_y, where "A" comprises at least one element which is selected from Group 13, Group 14, Group 15, or Group 17 of the periodic table. A silver comprising layer is formed over the chalcogenide material. The silver is irradiated effective to break a chalcogenide bond of the chalcogenide material at an interface of the silver comprising layer and chalcogenide material and diffuse at least some of the silver into the chalcogenide material, and an outer surface of the chalcogenide material is formed. After the irradiating, the chalcogenide material outer surface is exposed to an iodine comprising fluid effective to reduce roughness of the chalcogenide material outer surface from what it was prior to the exposing. After the exposing, a second conductive electrode material is deposited over the chalcogenide material, and which is continuous and completely covering at least over the chalcogenide material, and the second conductive electrode material is formed into an electrode of the device.

Other implementations and aspects are contemplated and disclosed.

BRIEF DESCRIPTION OF THE DRAWINGS

Preferred embodiments of the invention are described below with reference to the following accompanying drawings.

Fig. 1 is a diagrammatic sectional view of a semiconductor wafer fragment in process in accordance with an aspect of the invention.

Fig. 2 is a view of the Fig. 1 wafer fragment at a processing step subsequent to that shown by Fig. 1.

Fig. 3 is a view of the Fig. 1 wafer fragment at a processing step subsequent to that shown by Fig. 2.

Fig. 4 is a view of the Fig. 1 wafer fragment at a processing step subsequent to that shown by Fig. 3.

Fig. 5 is a view of the Fig. 1 wafer fragment at a processing step subsequent to that shown by Fig. 4.

Fig. 6 is a view of the Fig. 1 wafer fragment at a processing step subsequent to that shown by Fig. 5.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

This disclosure of the invention is submitted in furtherance of the constitutional purposes of the U.S. Patent Laws "to promote the progress of science and useful arts" (Article 1, Section 8).

Referring to Fig. 1, a semiconductor wafer fragment 10 is shown in but one preferred embodiment of a method of forming a non-volatile resistance variable device. By way of example only, example such devices include programmable metallization cells and programmable optical elements of the patents referred to above, further by way of example only, including programmable capacitance elements, programmable resistance elements, programmable antifuses of integrated circuitry and programmable memory cells of memory circuitry. The above patents are herein incorporated by reference. The invention contemplates the fabrication techniques and structure of any existing non-volatile resistance variable device, as well as yet-to-be developed such devices. In the context of this document, the term "semiconductor substrate" or "semiconductive substrate" is defined to mean any construction comprising semiconductive material, including, but not limited to, bulk semiconductive materials such as a semiconductive wafer (either alone or in assemblies comprising other materials thereon), and semiconductive material layers (either alone or in assemblies comprising other materials). The term "substrate" refers to any supporting structure, including, but not limited to, the semiconductive substrates described above. Also in the context of this document, the term "layer" encompasses both the singular and the plural unless

otherwise indicated. Further, it will be appreciated by the artisan that "resistance variable device" includes devices wherein a property or properties in addition to resistance is/are also varied. For example, and by way of example only, the device's capacitance and/or inductance might also be changed in addition to resistance.

Semiconductor wafer fragment 10 comprises a bulk monocrystalline semiconductive material 12, for example silicon, having an insulative dielectric layer 14, for example silicon dioxide, formed thereover. A first conductive electrode material 16 is formed over dielectric layer 14. By way of example only, preferred materials include any of those described in the incorporated Kozicki et al. patents referred to above in conjunction with the preferred type of device being fabricated. A dielectric layer 18 is formed over first electrode material 16. Silicon nitride is a preferred example.

An opening 20 is formed through layer 18 to conductive electrode layer 16. Such is filled with a chalcogenide comprising material 22 to a first thickness, which in this example is essentially defined by the thickness of layer 18. By way of example only, an exemplary first thickness range is from 100 Angstroms to 1000 Angstroms. The chalcogenide comprising material comprises A_xSe_y, where "A" comprises at least one element which is selected from Group 13 (B, Al, Ga, In, Tl), Group 14 (C, Si, Ge, Sn, Pb), Group 15 (N, P, As, Sb, Bi), or Group 17 (F, Cl, Br, I, At) of the periodic table. By way of example only, preferred elements for "A" are Ge and Si. An example preferred method of forming material 22 over substrate 10 is by chemical vapor

deposition to completely fill opening 20, followed by a planarization technique, for example chemical mechanical polishing. Material 22 is preferably formed to be amorphous and remains amorphous in the finished device.

A silver comprising layer 24 is formed to a second thickness over chalcogenide material 22. Silver comprising layer 24 is preferably predominately (majority) elemental silver, and can consist or consist essentially of elemental silver. In one preferred embodiment, the second thickness is at least 30% of the first thickness.

Referring to Fig. 2, silver comprising layer 24 is irradiated effective to break the chalcogenide bond of chalcogenide material 22 at an interface of silver comprising layer 24 and chalcogenide material 22, and diffuse at least some of the silver into chalcogenide material 22. In Fig. 2, material 22 is designated with numeral 23 and peppered in the drawing to indicate metal ions being received therein. A preferred irradiating includes exposure to actinic radiation having a wavelength from about 164 - 904 nanometers, with radiation exposure at between 404 - 408 nanometers being a more specific example. A more specific example is a flood UV exposure tool operating at 4.5 milliwatts/cm^2 energy for 15 minutes in an oxygen-containing ambient at room temperature and pressure. All of material 24 received directly over chalcogenide comprising material 22 might be diffused to within such material, or only some portion thereof might. The thickness of layer 24 is also chosen to be suitably thin to enable the impinging electromagnetic radiation to essentially transparently pass through material 24 to the interface of such material with chalcogenide

material 22. An exemplary preferred thickness is less than or equal to 200 Angstroms. Further, the apparent linear thickness of layer 24 as a percentage of the linear thickness of chalcogenide material 22 effectively results in the same approximate metal incorporation in atomic percent within the chalcogenide material. Regardless, such results in chalcogenide material 23 having an outer surface 25.

In but one embodiment, outer surface 25 is characterized by the formation of Ag_2Se as at least part of the outer surface, with in one embodiment, the irradiating being effective to form a discontinuous layer 27 of Ag_2Se formed over chalcogenide comprising materials 22/23. Further preferably, the irradiating is effective to maintain the chalcogenide material underlying the Ag_2Se in a substantially amorphous state. Even further preferably, the irradiating is effective to dope the chalcogenide comprising material to average at least 30 atomic percent silver in a lowest of a plurality of variable resistant states. Further, the invention contemplates any other method of forming Ag_2Se over chalcogenide comprising material, and for example a discontinuous layer of Ag_2Se, by any other existing or yet-to-be-developed methods.

Referring to Fig. 3 and after the irradiating, chalcogenide material outer surface 25 is exposed to an iodine comprising fluid effective to reduce roughness of chalcogenide material outer surface 25 from what it was prior to the exposing. In one preferred embodiment, such exposing occurs to Ag_2Se to be effective to etch away at least some of the Ag_2Se, more preferably effective to etch away at least a majority of the Ag_2Se, and most preferably

effective to etch away substantially all of the Ag_2Se, as shown in Fig. 3. In one exemplary embodiment, roughness reduction is contemplated independent of Ag_2Se formation and removal. Further in one exemplary embodiment, etching away of at least some Ag_2Se is contemplated independent of the effect on surface roughness.

One preferred iodine comprising fluid is a liquid, for example an iodide solution such as a potassium iodide solution. An example preferred potassium iodide solution comprises from 5 to 30 grams of I_2 per one liter of a from 20% to 50% by volume potassium iodide solution. Exposure to a vapor, a liquid solution at for example ambient temperature and pressure conditions, or elevated or reduced from ambient temperature and/or pressure conditions is of course also contemplated. A specific example is dipping the substrate into a potassium iodide solution comprising 20 grams of I_2 per one liter of a 30% potassium iodide solution.

Referring to Fig. 4 and after the exposing, a second conductive electrode material 26 is deposited over chalcogenide material 23. In the preferred embodiment, such second conductive electrode material is continuous and completely covers at least over chalcogenide material 23. An example preferred thickness range for second electrode material 26 is from 140 Angstroms to 200 Angstroms. The first and second conductive electrode materials might be the same material(s), or different material(s). By way of example only, preferred top and bottom electrode materials include silver, tungsten, platinum, nickel, carbon, chromium, molybdenum, aluminum, magnesium, copper, cobalt, palladium,

vanadium, titanium, alloys thereof and compounds including one or more of these elements. In accordance with a preferred programmable metallization cell embodiment, and where "A" is Ge, at least one of materials 16 and 26 constitutes silver. During the formation of layer 26, some of it might diffuse into layer 23.

Referring to Fig. 5, material 26 is patterned into an electrode 30. Patterning to produce electrode 30 is typically and preferably conducted utilizing photolithography. Such provides but one preferred example of forming a second electrode material operatively proximate the chalcogenide material. In a preferred embodiment, such results in the formation of a non-volatile resistance variable device which is fabricated into a programmable memory cell of memory circuitry.

Referring to Fig. 6, one or more dielectric layers 32 are ultimately formed over the device. Of course, intervening conductive and semiconductive layers might also be provided to form other lines and devices outwardly of the depicted device.

In compliance with the statute, the invention has been described in language more or less specific as to structural and methodical features. It is to be understood, however, that the invention is not limited to the specific features shown and described, since the means herein disclosed comprise preferred forms of putting the invention into effect. The invention is, therefore, claimed in any of its forms or modifications within the proper scope of the

appended claims appropriately interpreted in accordance with the doctrine of equivalents.